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10/761,048	01/20/2004	Stephen R. Van Doren	200313612-1	1168

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EXAMINER	
ALI, FARHAD	

ART UNIT	PAPER NUMBER
2146	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/761,048	VAN DOREN ET AL.	
	Examiner	Art Unit	
	FARHAD ALI	2146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Rowlands (US 6,993,631 B2).

Rowlands teaches:

Claim 1

A system comprising:

a first node that broadcasts a request for data; and

a second node having a first state associated with the data that defines the second node as an ordering point for the data, the second node providing a response to the first node that transfers the ordering point to the first node in response to the request for the data **(A first node includes a first cache and a plurality of coherent agents. In response to a transaction to a coherency block by a first coherent agent of the plurality of coherent agents, the first node is configured to fetch the coherency block from another node. The other node is configured to record a state in which**

the coherency block is provided to the first node. The first cache is designated to store the state of the coherency block recorded by the first node [abstract] and see Column 21 Lines 27-43, ownership).

Claim 2

The system of claim 1, wherein the first node transitions to a second state associated with the data in response to receiving the response from the second node, the second state defining the first node as the ordering point for the data **(The other node is configured to record a state in which the coherency block is provided to the first node. The first cache is designated to store the state of the coherency block recorded by the first node [abstract])**.

Claim 3

The system of claim 2, wherein the second state corresponds to a state of a cache line that contains the data, the second state enabling the first node to provide an ownership data response that includes a copy of the data to requests for the data **(Column 2, Lines 4-11 "A first coherency block is fetched from a first node into a second node. The second node includes a first cache and a plurality of coherent agents. The first cache is accessible to the plurality of coherent agents. A state is retained in the first cache for the first coherency block. The state is recorded by the first node for the first coherency block and is the state in the second node. The cache is designated to retain the state")**.

Claim 4

The system of claim 2, wherein the first node comprises a processor having an associated cache that comprises plurality of cache lines, one of the cache lines having an address associated with the data, the second state identifying the one of the cache lines as the ordering point for the data in the system **(Column 2, Lines 4-11 "A first coherency block is fetched from a first node into a second node. The second node includes a first cache and a plurality of coherent agents. The first cache is accessible to the plurality of coherent agents. A state is retained in the first cache for the first coherency block. The state is recorded by the first node for the first coherency block and is the state in the second node. The cache is designated to retain the state")**.

Claim 5

The system of claim 1, wherein the second node transitions from the first state to a transition state associated with migration of the ordering point to the first node **(Column 12-13, Lines 66-3, "The exclusive and modified states may be treated the same in the response phase in this embodiment, and the exclusive/modified owner may provide the data. The exclusive/modified owner may provide, concurrent with the data, an indication of whether the state is exclusive or modified")**.

Claim 6

The system of claim 5, wherein the second node comprises a processor having an associated cache that comprises a plurality of cache lines, one of the cache lines of the second node that contains the data transitioning from the first state to the transition state associated with migration of the ordering point to the first node **(Column 12-13, Lines 66-3, "The exclusive and modified states may be treated the same in the response phase in this embodiment, and the exclusive/modified owner may provide the data. The exclusive/modified owner may provide, concurrent with the data, an indication of whether the state is exclusive or modified")**.

Claim 7

The system of claim 5, further comprising a multi-processor system implementing a source broadcast protocol, the system further comprising a third node that issues a broadcast request that is received at the second node while in the transition state, the third node reissuing the broadcast request as a request employing an associated forward progress protocol implemented in the system in response to receiving a conflict response from the second node **(Column 22 Lines 16-33, address transfer may be retried, or cancelled (e.g.g to permit a modified cache block to be written to memory, or other coherency activity to occur))**.

Claim 8

The system of claim 7, wherein the forward progress protocol comprises a directory-based protocol **(Column 4 Lines 24-37, "The remote line directory 34 may be used in the home node to track the state of the local cache blocks in the remote nodes. The remote line directory 34 is updated each time a cache block is transmitted to a remote node, the remote node returns the cache block to the home node, or the cache block is invalidated via probes. As used herein, the "state" of a cache block in a given node refers to an indication of the ownership that the given node has for the cache block according to the coherency protocol implemented by the nodes. Certain levels of ownership may permit no access, read-only access, or read-write access to the cache block. For example, in one embodiment, the modified, shared, and invalid states are supported in the internode coherency protocol")**.

Claim 9

The system of claim 1, wherein the first node provides an acknowledgment signal to the second node after receiving responses from other nodes in the system **(Column 10-11 Lines 65-2, "The probe commands are responded to (after effecting the state changes requested by the probe commands) using either the Kill_Ack or WB commands. The Kill_Ack command is an acknowledgement that a Kill command has been processed by a receiving node")**.

Claim 10

The system of claim 9, wherein the second node provides a signal to the first node indicating receipt of the acknowledgement signal **(Column 13 Lines 31-33, "The memory bridge 32 may signal the memory controller 14/L2 cache 36 when the acknowledgements have been received")**.

Claim 11

The system of claim 1, wherein the request for the data comprises a request for the data requiring write permission **(Column 9 Lines 47-60, write transaction)**.

Claim 12

The system of claim 11, wherein the request for the data further comprises one of a source broadcast read request or a source broadcast write request for the data, and the response from the second node comprises a corresponding ownership data response **(Column 9 Lines 47-60, write transaction)**.

Claim 13

The system of claim 1, wherein each of the first and second nodes comprises a processor having an associated cache that comprises a plurality of cache lines, each cache line having a respective address that identifies associated data and state information that identifies a state of the associated data for the respective cache line, each of the processors being capable of communicating with each other via an interconnect **(Column 2 Lines 12-20, "In another embodiment, a node comprises a**

plurality of first level caches configured to store cache blocks and corresponding states and a second level cache. The second level cache is configured to store cache blocks and corresponding states. A remote cache block is stored in the second level cache and the corresponding state in the second level cache is the state recorded by a home node of the remote cache block for the node" and Figure 1 see Processor and Interconnect).

Claim 14

The system of claim 13, wherein each processor further comprises a cache controller that controls the state of the data stored in the plurality of cache lines thereof, at least the cache controller of the first node further comprises a state engine capable of modifying the state information for the cache line associated with the data to a state that defines the cache line associated with the data as the ordering point based on the response provided by the second node **(See Figure 1 Memory controller and claim 1 rejection).**

Claim 15

A computer system, comprising: a source processor that issues a broadcast request for desired data while having a first state associated with the desired data; and an owner processor having an associated cache that includes the desired data in a cache line, the cache line having an associated state that defines a copy of the desired data as an ordering point for the desired data, the owner processor responding to the

broadcast request with an ownership data response that includes the desired data, the source processor transitioning from the first state to a second state associated with the desired data based on the ownership data response, the second state defining the source processor as the ordering point for the desired data **(A first node includes a first cache and a plurality of coherent agents. In response to a transaction to a coherency block by a first coherent agent of the plurality of coherent agents, the first node is configured to fetch the coherency block from another node. The other node is configured to record a state in which the coherency block is provided to the first node. The first cache is designated to store the state of the coherency block recorded by the first node [abstract] and see Column 21 Lines 27-43, ownership)**.

Claim 16

The system of claim 15, wherein the source processor further comprises a cache line that contains the desired data received from the owner processor, the cache line of the source processor that contains the desired data having an associated state that transitions to a second state in response to receiving the ownership data response from the owner processor, the second state defining the cache line of the source processor that contains the desired data as the ordering point for the data **(The other node is configured to record a state in which the coherency block is provided to the first node. The first cache is designated to store the state of the coherency block recorded by the first node [abstract] and see claim 15 rejection)**.

Claim 17

The system of claim 16, wherein the second state enables the source processor to respond to requests for the desired data by providing an ownership data response that includes a copy of the desired data **(Column 2, Lines 4-11 "A first coherency block is fetched from a first node into a second node. The second node includes a first cache and a plurality of coherent agents. The first cache is accessible to the plurality of coherent agents. A state is retained in the first cache for the first coherency block. The state is recorded by the first node for the first coherency block and is the state in the second node. The cache is designated to retain the state")**.

Claim 18

The system of claim 17, wherein the state associated with the cache line of the owner processor transitions from a first state to a transition state in connection with providing the ownership data response to the source processor **(Column 2, Lines 4-11 "A first coherency block is fetched from a first node into a second node. The second node includes a first cache and a plurality of coherent agents. The first cache is accessible to the plurality of coherent agents. A state is retained in the first cache for the first coherency block. The state is recorded by the first node for the first coherency block and is the state in the second node. The cache is designated to retain the state")**.

Claim 19

The system of claim 18, wherein the system employs a source broadcast protocol for controlling the broadcast request issued by the source processor and the response provided by the owner processor, the system further comprising a third processor that issues a broadcast request using the source broadcast protocol that is received at the owner processor while in the transition state, the third processor reissuing the request employing an associated forward progress protocol implemented in the system in response to receiving a conflict response from the owner processor **(Column 22 Lines 16-33, address transfer may be retried, or cancelled (e.g.g to permit a modified cache block to be written to memory, or other coherency activity to occur))**.

Claim 20

The system of claim 19, wherein the forward progress protocol comprises a directory-based protocol **(Column 4 Lines 24-37, "The remote line directory 34 may be used in the home node to track the state of the local cache blocks in the remote nodes. The remote line directory 34 is updated each time a cache block is transmitted to a remote node, the remote node returns the cache block to the home node, or the cache block is invalidated via probes. As used herein, the "state" of a cache block in a given node refers to an indication of the ownership that the given node has for the cache block according to the coherency protocol**

implemented by the nodes. Certain levels of ownership may permit no access, read-only access, or read-write access to the cache block. For example, in one embodiment, the modified, shared, and invalid states are supported in the internode coherency protocol").

Claim 21

The system of claim 15, wherein the source processor provides an acknowledgment signal to the owner processor after receiving a complete set of responses from the system, the acknowledgement signal enabling the owner processor to transition from a transition state to an invalid state **(Column 10-11 Lines 65-2, "The probe commands are responded to (after effecting the state changes requested by the probe commands) using either the Kill_Ack or WB commands. The Kill_Ack command is an acknowledgement that a Kill command has been processed by a receiving node")**.

Claim 22

The system of claim 21, wherein the owner processor provides a signal to the source processor indicating receipt of the acknowledgement signal signal **(Column 13 Lines 31-33, "The memory bridge 32 may signal the memory controller 14/L2 cache 36 when the acknowledgements have been received")**.

Claim 23

The system of claim 15, wherein the owner processor provides a blocking signal to prevent a home node from responding with a copy of the desired data in response to receiving the broadcast request from the source processor **(Column 20 Lines 54-63, "In other embodiments, the interconnect 22 may support a source blocking scheme in which each agent that participates in various transactions may supply a block signal that is asserted to indicate whether or not it is capable of participating in a transaction of a given type, if it were to be transmitted on the interconnect 22. Each agent that sources transactions may receive the block signals, and may inhibit initiating a transaction if an agent that is to participate in that transaction, when initiated on the interconnect 22, has its block signal asserted")**.

Claim 24

A system, comprising: means for broadcasting a request for data from a first processor node having a cache state associated with the requested data; means for providing an ownership data response from a second processor node having a cache state that defines the second processor as a cache ordering point for the requested data; and means for transferring the cache ordering point from the second processor node to the first processor node associated with the first processor node receiving the ownership data response from the second processor node **(A first node includes a first cache and a plurality of coherent agents. In response to a transaction to a coherency block by a first coherent agent of the plurality of coherent agents, the**

first node is configured to fetch the coherency block from another node. The other node is configured to record a state in which the coherency block is provided to the first node. The first cache is designated to store the state of the coherency block recorded by the first node [abstract] and see Column 21 Lines 27-43, ownership).

Claim 25

The system of claim 24, further comprising means for providing a migration acknowledgment signal to acknowledge receipt of the ownership data response at the first processor node and for transitioning to a cache state at the first processor node that defines the first processor node as the cache ordering point **(The other node is configured to record a state in which the coherency block is provided to the first node. The first cache is designated to store the state of the coherency block recorded by the first node [abstract] and see claim 24 rejection)**.

Claim 26

The system of claim 25, further comprising means for acknowledging receipt of the migration acknowledgment signal by the second processor node **(Column 10-11 Lines 65-2, "The probe commands are responded to (after effecting the state changes requested by the probe commands) using either the Kill_Ack or WB commands. The Kill_Ack command is an acknowledgement that a Kill command has been processed by a receiving node")**.

Claim 27

The system of claim 24, wherein each of the means for broadcasting, the means for providing and the means for transferring employs a source broadcast protocol, the system further comprising means for reissuing a request in the system using a forward progress protocol in response to detecting a conflict while employing the source broadcast protocol **(Column 22 Lines 16-33, address transfer may be retried, or cancelled (e.g.g to permit a modified cache block to be written to memory, or other coherency activity to occur))**.

Claim 28

A method comprising: broadcasting from a source node a request for requested data; providing an ownership data response from an owner node in response to the request from the source node; and transitioning a state at the source node associated with the requested data from a first state to a second state in response to receiving the ownership data response, the second state defining the source node as a new cache ordering point **(A first node includes a first cache and a plurality of coherent agents. In response to a transaction to a coherency block by a first coherent agent of the plurality of coherent agents, the first node is configured to fetch the coherency block from another node. The other node is configured to record a state in which the coherency block is provided to the first node. The first cache is**

designated to store the state of the coherency block recorded by the first node [abstract] and see Column 21 Lines 27-43, ownership).

Claim 29

The method of claim 28, further comprising providing a migration acknowledgment signal from the source node to acknowledge receipt of the ownership data response at the source node **(Column 10-11 Lines 65-2, "The probe commands are responded to (after effecting the state changes requested by the probe commands) using either the Kill_Ack or WB commands. The Kill_Ack command is an acknowledgement that a Kill command has been processed by a receiving node")**.

Claim 30

The method of claim 29, further comprising: entering a transition state at the owner node in response to providing the ownership data response; and releasing the owner node from the transition state in response to the migration acknowledgment signal **(The other node is configured to record a state in which the coherency block is provided to the first node. The first cache is designated to store the state of the coherency block recorded by the first node [abstract] and see claim 28 rejection)**.

Claim 31

The method of claim 30, wherein the source node and the owner node employ a source broadcast protocol, the method further comprising: issuing a broadcast request for the requested data from a third node using the source broadcast protocol; and reissuing the broadcast request from the third node as a request using a forward progress protocol in response to the owner node being in the transition state 1 when the owner node receives the broadcast request issued by the third node **(Column 22 Lines 16-33, address transfer may be retried, or cancelled (e.g.g to permit a modified cache block to be written to memory, or other coherency activity to occur))**.

Claim 32

The method of claim 29, further comprising providing an acknowledgment signal to the source node to acknowledge receipt of the migration acknowledgment signal at the owner node **(Column 13 Lines 31-33, "The memory bridge 32 may signal the memory controller 14/L2 cache 36 when the acknowledgements have been received")**.

Claim 33

The method of claim 28, wherein the source node comprises a processor node that includes a cache having a plurality of cache lines, one of the cache lines of the processor node containing the requested data based on the ownership data response and having a state associated therewith, the state associated with the one of the cache lines defining the source node as the new cache ordering point **(Column 2 Lines 12-20,**

"In another embodiment, a node comprises a plurality of first level caches configured to store cache blocks and corresponding states and a second level cache. The second level cache is configured to store cache blocks and corresponding states. A remote cache block is stored in the second level cache and the corresponding state in the second level cache is the state recorded by a home node of the remote cache block for the node" and Figure 1 see Processor and Interconnect).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FARHAD ALI whose telephone number is (571)270-1920. The examiner can normally be reached on Monday thru Friday, 7:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey C. Pwu can be reached on (571) 272-6798. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Farhad Ali/
Examiner, Art Unit 2146

/Jeffrey Pwu/
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